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Analytical Model of Tunneling Current by High Dielectrics and Study of High-k Gate Stack Structure

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Abstract: *With the persistent scale of dielectrics through scaling technology towards the nanoscale method and a precise model of tunnel current becomes important as well as essential to understand the scaling limits. While precised by (ITRS) and elevated presentation CMOS circuit has the utmost current density limit for 90 nm skill nodes. Below 2nm oxide tunneling current becomes difficult. Classical physics is not enough to explain the device physics at nanoscale. So a quantum mechanical study becomes essential to provide thorough evaluation of the device behavior at nanoscale. By solving Schrödinger Equation, analytical model for gate tunneling current has been urbanized using (WKB) approximation method. The tunneling current has been calculated for direct tunneling from channel to gate for both electrons and holes. To avoid the problem of gate tunneling current below 90 nm or we can say that at 65 nm and 45 nm another gate dielectric material is used that has high dielectric constant than* SiO_2. *Three gate dielectric materials* Si_3N_4, HfO_2, Al_2O_3 *has been deliberated .All the three gate dielectrics are used to scale down the thickness of oxide ranging from 1.42 nm to 0.96 nm. Results have been compared with the numerical model and also with the semi-empirical model.*

Key words: *direct tunneling; gate current; gate dielectric; gate stack, nanoscale MOSFET*

I. INTRODUCTION

MOSFET (Metal Oxide Semiconductor Field Effect Transistor) technology is the fortitude of the semiconductor industry over the last three decades. Two factors is necessary for the technology to be that doing well. First it has to provide rapid improvement in product performance and second the cost of new product has to be kept low to widen the collection of potential customer. The reduction in size of MOSFET transistor has helped to meet both of these goals. As the transistor gate length reduces the amount of current supplied by a transistor increases. Higher current allowed the circuit to switch more quickly and leads to faster calculation. The reduction in transistor size also allowed more transistors must be integrated on a circuit. Thus complexity of integrated circuit can be increased while keeping the cost of circuit production low.

II. ISSUES OF DEVICE SCALING

The fundamental purpose of FET in digital circuit is to operate as a switch i.e. when large voltage is functional to gate it allows electric current to flow as of source to drain and when low voltage is applied to the gate it blocks the current. The ability to conduct current depends on the electric potential in the body of a transistor. This potential is in turn determined by the amount of capacitive coupling between the transistor body and various electrodes.In long channel device the gate has exclusive control over the middle region of the body and can therefore effectively cut off the conduction. Though if the device length is reduced the section where the potential are controlled through source/drain,the electrodes eventually merge and the gate electrode will no longer be able to successfully block the current conduction[1-3].In order to improve the gate control the thickness of SiO_2 dielectric should be reduced which is shown in Fig.1. There are some reason to follow efficiency includes: (a) as MOSFET occupy small region so the price per transistor must be decreased (b) many transistor may be included in the circuit consequently it perform many multiple function (c) capacitance is decreased that decreases instant and influence needed to control MOSFET.

Although the potential benefits efficiency present a sequence of challenge to the device designs. First the power utilization of system enhances significantly at large frequency action. Hence the heat production through high frequency Si circuit is extremely large the cooling of circuit becomes tricky and on occasion sensibly impractical intended for small power application. Supply voltage drop is an efficient technique to deduce the power consumption per device. Lessing of supply voltage deduces the prepared pace of MOSFET.

Thus scheming of power utilization has become a chief alarm in MOSFET scaling. It has been originated to keep the operational pace of MOSFET. Thethreshold voltage Vth must be deduced at the same speed at which the supply voltage is decreased. Therefore the low Vth leads to extreme sub threshold leakage current in MOSFET.

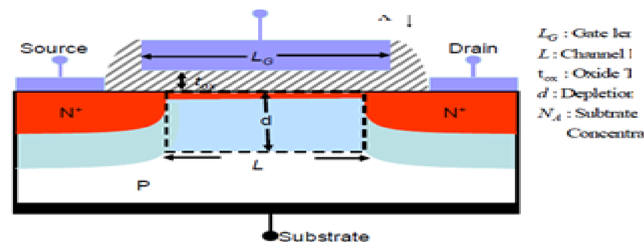

Fig1: Structure of bulk MOSFET

By decreasing oxide layer thickness (tox) the threshold voltage is reduced in a mass MOSFET that cause leakage from the gate oxide. Therefore the connection between power utilization and operational pace is significant to obtain most favorable scaled tool. Second a MOSFET feature degrades with the lessening in dimension. There are two main feature that is Vth and sub threshold swing, S recognized as short channel effect (SCE)[4].For down scaling the length of channel lacking extreme SCE both the oxide thickness, tox and the gate controlled depletion depth, d must be abridged. Correspond to 6 atomic layers of Si oxide the oxide thickness is 1.2 nm for 90 nm technology. More reducing oxide thickness becomes more and more difficult and grounds the critical leakage of gate.

Lastly the classical physics becomes inadequate to recognize completely the behavior of MOSFET at little size. The channel length of upcoming MOSFET becomes imminent and the representing path between carrier collision and the thickness of oxide layer reaches the height of little atomic layer. In these circumstances the major divergence from the classical calculation is watched in the behavior of MOSFET that must be explained by quantum theory. As MOSFET are scaled down with giga scale integration (GSI) and quantum effects are required and considered in MOSFET model and designing [5]. In CMOS technology the gate oxide thickness of MOSFET is less than 1.5 nm and the doping of channel is high as 1e18cm-3 [6-8]. Occurring of tunneling at drain/source porch area overlaps with the gate as shown in Fig.2. Also band-to-band tunneling (BTBT) occurring is due to electron cross a reverse bias pn junction from p-side valence band to n-side conduction band.

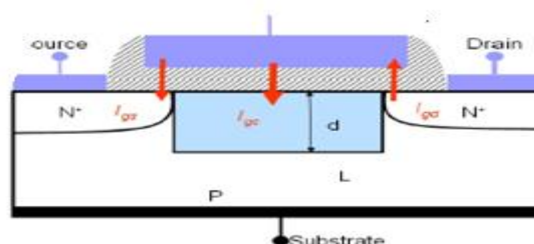

Fig 2: Tunneling current in a MOSFET

III. MODELING APPROACH

Modeling of tunneling current through gate dielectrics is done by many approches. Generally we use three approaches -

- Numerical model
- Semi-empirical model
- Analytical model

Numerical model-

-Bardeen Approach
-Resonant transfer matrix method
-Transparency based approximation

Semi-empirical model-

-Provides excellent accuracy for particular frame of work.

Analytical model-

-WKB approximation

3.1 High-k gate Dielectrics

For controlling and avoiding the reliability concern of the direct tunneling current of gate dielectrics the physical thickness must be enhanced. Though ultra thin silicon oxide layer is consumed to produce high electrical field in vertical direction to control SCE and guarantee for sufficient drive current in bulk MOSFET [9,10]. Therefore the electrical width of gate dielectrics should be reduced and physical width must be constant. The simply solution is replace the SiO2 with high-k material for gate insulation. Among diverse high-k material Al_2O_3, La_2O_3, HfO2, HfSiO4 emerge to be the candidate to replace SiO2. These high-k materials show the style of reducing the height of barrier with increasing dielectric constant. For high-k material an equivalent oxide thickness, EOT can be inserted which defines the equivalent thickness of Si oxide desirable to obtain the same gate capacitance as the one obtained by high-k dielectrics.

$$EOT = 3.9 \frac{t_{high\text{-}k}}{k_{high\text{-}k}}$$

where $k_{high\text{-}k}$ and $t_{high\text{-}k}$ are the dielectric constant and physical width of high-k materials. Fig.3 shows the imitation outcome to show the reduction of tunneling current density with the consumption of high-k materials [11]. In MOSFET the gate dielectrics co-operate the role of a potential barrier sorting out carriers from gate in the channel. With a broad dielectric layers the wave function of carriers cannot expand to the gate by piercing the potential barrier [12]. Though in MOSFET scaling the width of dielectrics should be reduced beside with the channel length to enhance and avoids the control of gate and short channel effects and transconductance squalor.

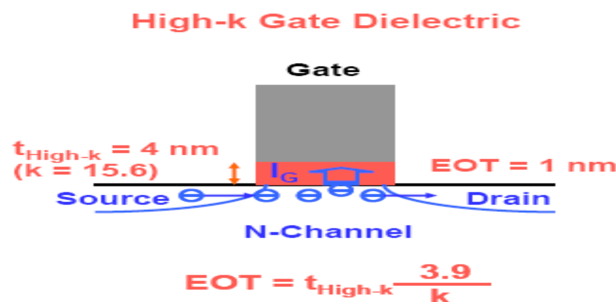

Fig.3: Schematic showing EOT

Energy band diagram for high-k dielectrics-

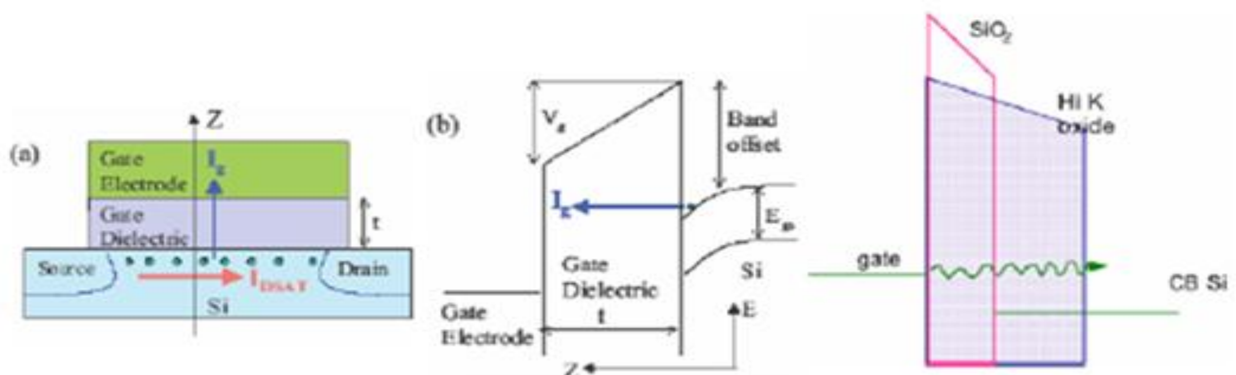

Fig 4:(a) Graphic cross section of n-channel transistor along with its channel and the green dot in the transistor channel illustrate the carrier of charge (b) in the direction perpendicular to channel corresponds to energy band diagram and Vg is applied gate bias (c) Schematic direct tunneling through a SiO_2 layer and the more difficult tunneling through thicker layer of high-k oxide [13].

IV. TUNNELING THEORY

The thickness of the potential barrier is an important factor to conclude the tunneling probability acc. to tunneling theory .The quantum mechanical thought state that all matters include electron behave likes both particle as well as wave. The quantum mechanical investigation in which wave nature of electron is emphasizing and becomes essential if the magnitude of the potential is comparable to the wavelength of deBroglie of electrons that is $\lambda = h/\sqrt{(3m^{*}kT)}$. At room temperature deBroglie wavelength is approximately 1.5nm [14]. Modern MOSFET near the interface with thin gate oxide has very thin potential well. These wells are constructed by the barrier of oxide and the conduction band if Si that bend down penetratingly towards the surface as shown in Fig. 5(a).In the inversion layer carrier are restricted very close to Si surface near the potential well .In discrete subbands the energy level of electron are grouped and in normal direction it corresponds to quantized level. The nature of electron distribution in inversion layer differs if electrons are represented as wave function and significantly the electrons are treated as classical particle [15] which is shown in Fig. 5(b). The basic difference of quantum theory from classical physics is that infinitely small particle is treated as wave [16]. Contrasting the 'solid billiards' with definite position and velocity is assumed in classical theory and particle in quantum theory are waves detached in space. This quantum mechanical description of the particle is represented by the wave function $\psi(r)$ and the probability of finding the particle in the volume dr^3 is equal to $|\psi\, r^2|dr^3$.

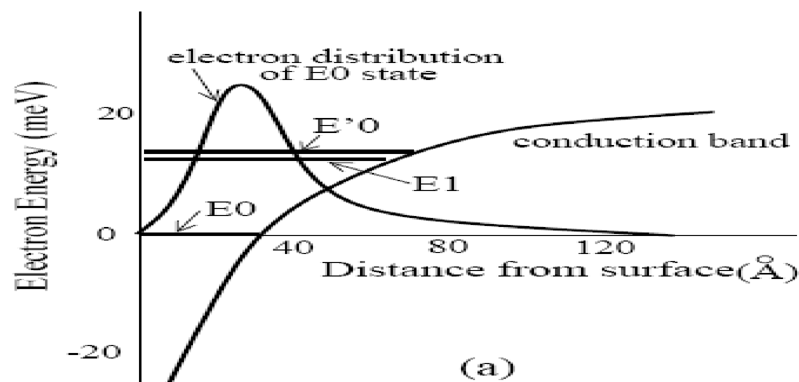

Fig.5 (a): Designing of Quantum mechanical band bending and concentration of electron distribution

The wave function is a mathematical tool that the quantum mechanics uses to explain any physical system. In a semiconductor the wave function of a carrier satisfies the Schrödinger equation. The Schrödinger in 1926 provides a formulation called wave mechanics by which the motion of electron in a crystal can be explained by wave theory. Particle can be explained by a wave function ψ (x, y, z) so that the probability of resulting the particle in the volume dxdydz is equal to $|\psi(x, y, z)|^2$ dxdydz. The wave function of electron satisfy the Schrödinger equation:

$$-\hbar^2/2m \nabla \psi(x, y, z) + U(x, y, z)\,\psi(x, y, z) = E\,\psi(x, y, z) \quad (1)$$

where $\hbar = h/2\pi$ is the Planck constant, m is the mass, E is the energy of particle and U is the potential energy. The study of tunneling should be based on the resolution of Schrödinger equation [17]. Fig.6 shows the simple case in which the energy of electron E with rectangular potential barrier is in the space and barrier height is Eb in eV and thickness is d in cm. In x direction, the Schrödinger equation is represented in different regions as follow-

$$d^2\psi / dx^2 + kI^2 \psi = 0 \quad \text{for } x < 0 \quad (2)$$
$$d^2\psi / dx^2 + k\,II^2 \psi = 0 \quad \text{for } 0 \le x \le d \quad (3)$$
$$d^2\psi / dx^2 + k\,III^2 \psi = 0 \quad \text{for } x \ge d \quad (4)$$

Where $kI^2 = k\,III^2 = 2mE/\hbar^2$

And $n_b^2 = (E - E_b)/ d$

The tunneling probability is given from the explanation of the Schrödinger equation-

$$D(E_x) = \exp\left(-\frac{2}{\hbar}\int_{x_1}^{x_2}\sqrt{2m_{ox}\left(E_b(x) - E_x\right)}dx\right) \quad (5)$$

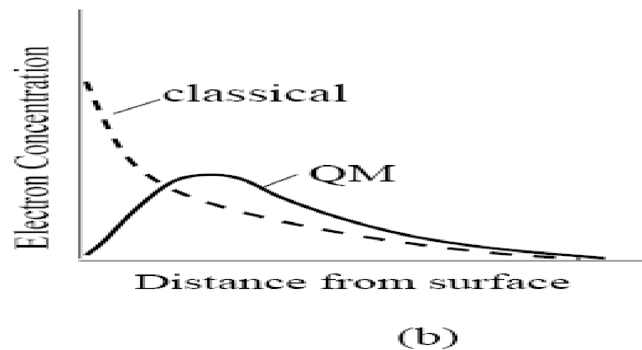

Fig.5 (b): Judgment between classical and Quantum Mechanical calculations of electron

Incident wave + Reflected wave **U(x)**

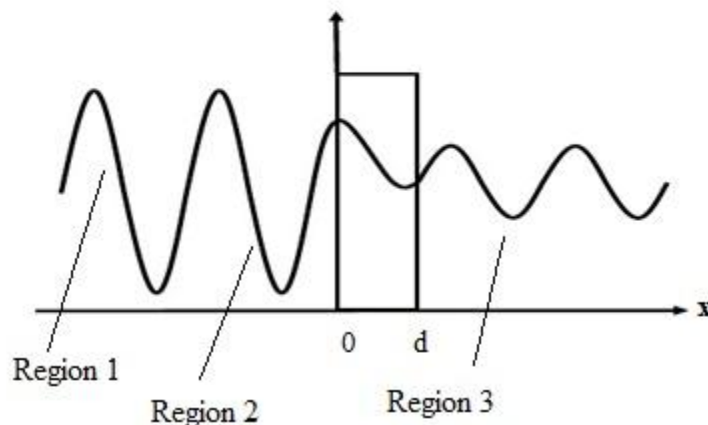

Fig.6: Tunneling of particle from the rectangular potential barrier of height Eb and thickness d

This formula shows that how to protect tunneling and the particles with higher kinetic energy and the larger values of height of barrier and the thickness are more likely to tunnel throughout the barrier.

V. CONCLUSION

In analytical model of gate tunneling current for MOSFET structure (n-MOSFET, p-MOSFET) is investigated. This analytical model is developed from the solution of Schrödinger Equation. Most difficult task is to find the tunneling probability through a trapezoidal potential barrier [18]. The probability of tunneling is computed with the help of WKB approach and equation of tunneling probability for an airy function has been used. A simulated result for gate tunneling current density is better matched for various gate dielectrics. For 90 nm technology thickness (tox) of SiO_2 is 1.5 nm observed so that the gate current density exceeds 1.0 A/cm^2 and we reduce the thickness of oxide below 1.5 nm and a large gate tunneling current drawn which causes maximum power dissipation. Hole tunneling current density is also calculated for p-MOSFET. Simulated results are shown for whole tunneling in p-MOSFET [19].Because of height of barrier is higher and the mass of the hole is largely

efficient. In p-MOSFET hole tunneling becomes lower than the electron tunneling in n-MOSFET. Metal gate in place of polysilicon gate for high-k material is required. Since there are several problems of using polysilicon gate for high-k gate dielectric materials first is polydepletion effect that increases the effective oxide thickness (EOT) that causes increase in the value of threshold voltage Vth and fall in the transconductance of the MOSFET [20].Therefore the Vth is required to enhance the semiconductor surface to maintain the inversion charge density and the second problem is Fermi-level pinning and phonon scattering that reduces the mobility.

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